Total No. of Printed Pages–8

ABP/CCM-25/XIV

ELECTRONICS

FIRST PAPER

Full Marks : 200

Time : 3 Hours

The figures in the margin indicate full marks for the questions.

Answer ***any ten*** *questions.*

1. *(a)* What is Fermi level in semiconductors? Write the equation for Fermi-Dirac distribution function and draw it for different temperatures for intrinsic semiconductors. 10

(b) Sketch the energy band diagram for

(i) *n*-type semiconductor

(ii) *p*-type semiconductor.

Indicate the positions of the Fermi level along with donor and acceptor levels. 5

Contd.

(c) What is base width modulation in BJT? Explain the phenomena. 5

2. (a) Deduce the *I-V* relationship for a Schottky barrier diode. 8

(b) Make a comparison of a Schottky barrier diode and the *p-n* junction diode on the basis of reverse saturation current densities and the switching characteristics. 6

(c) Calculate the forward-bias voltage required to generate a forward-bias current density of $10 A/cm^2$ in a Schottky barrier diode of tungsten barrier on silicon having barrier height of $0{\cdot}67 eV$ (Given effective Richardson constant $A^* = 114 A / K^2\text{-}cm^2$ & $T = 300 K$) 6

3. (a) List *three* sources of instability of collector current I_C in a BJT. How does the designer minimize the percentage variation in I_C *(i)* due to variation of I_{CO} and V_{BE} and *(ii)* due to variation in β? 3+5=8

(b)

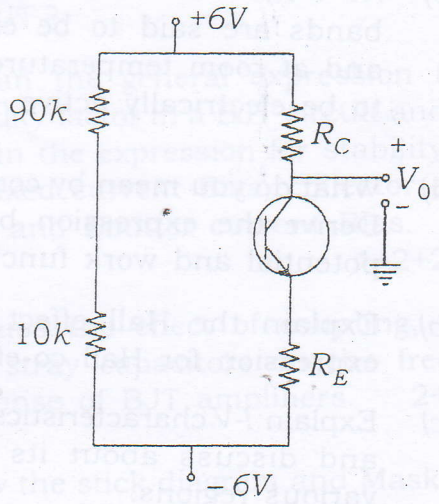

fig. 1

In the circuit shown in *fig.1* uses a transistor with β = 200 and is designed to make V_0=0 and V_{CE}=3V.

(i) Determine R_C and R_E

(ii) Using the values obtained in *(i)* find the change in V_0 given that β is halved.

(iii) The supply voltages each change by 5%. Determine the maximum change in V_0. Use the parameter values obtained in *(i)*. 12

4. *(a)* Obtain an expression for the density of allowed electron quantum states in terms of electron energy in the conduction band of semiconductor. 15

(b) At $0°K$, both conduction and valance bands are said to be electrically inert and at room temperature both are said to be electrically active — Why ? 5

5. (a) What do you mean by contact potential ? Derive the expression between contact potential and work function. 8

(b) Explain the Hall effect. Establish the expression for Hall co-efficient. 8

(c) Explain *I-V* characteristics of tunnel diode and discuss about its functioning in various regions. 4

6. (a) Describe *any one* practical method of growing an epitaxial layer on a wafer. 10

(b) Mention the most possible and commonly found defects in such crystal growth and suggest the ways to minimize these defects. 10

7. (a) Sketch the cross-section of a p-channel enhancement MOSFET. Draw the drain characteristics and transfer curve. 10

(b) Sketch the CMOS inverter circuit and explain its operation. What are the advantages of CMOS technology over PMOS and NMOS technologies ? 10

8. (a) What do you mean by thermal runaway in BJT? 4

(b) Obtain the general expression for the stability factor in a BJT circuit and hence obtain the expression for stability factor for fixed current Bias, collector to base Bias and Emitter current Bias. 4+2+2+2=10

(c) Discuss the effect of coupling, bypass and stray capacitors on the frequency response of BJT amplifiers. 2+2+2=6

9. (a) Draw the stick diagram and Mask layout for realization of the function $X = \overline{A + B + C}$ using lambda based design rule. 4+6=10

(b) Determine the pull-up to pull-down ratio for an nMOS inverter driven through one or more pass transistors. 10

10. (a) What is Standard Cell Library? Explain the design principle of a standard cell library. Does a full custom designer use a standard cell library? Justify your answer. 12

(b) Draw stick diagram for a CMOS circuit implementing three input NOR function. 8

11. *(a)* What are the *four* basic ways of connecting a feedback signal? Explain each with necessary block diagram. 10

(b)

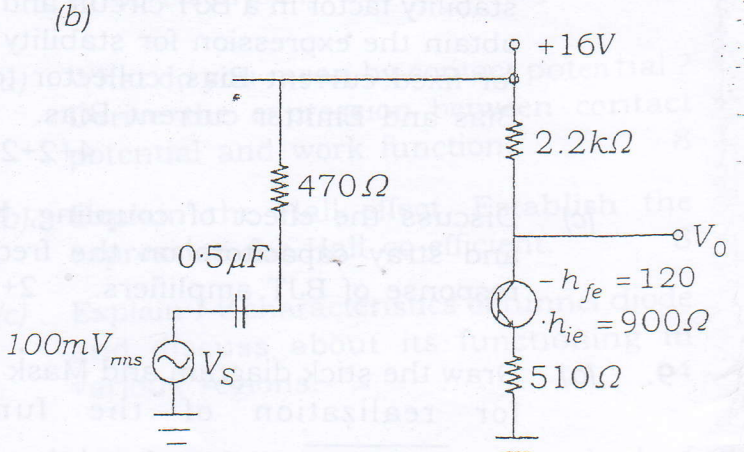

Fig. 2

What type of feedback is applied in the circuit shown in *Fig. 2*? For the circuit, calculate the voltage gain with and without feedback. 10

12. *(a)* Draw the Flowchart for finding out the average of 100 data elements stored in an Array. 8

(b) Discuss about various symbols used in Flowcharts along with their diagrams. 4

(c) If the content of the accumulator is 72*H*, what is the effects of executing the following instructions on the contents of accumulator and the flags *(any four)* :

(i) *XRA A* (ii) *ANI OFH*

(iii) *ORI 80H* (iv) *ORA A*

(v) *ADD A* (vii) *NOP*

2×4=8

13. (a) Discuss the interfacing of USART 8251 with 8085 microprocessor (μp) for serial data communication. 10

(b) Distinguish between memory read and write operations of 8085μp with appropriate timing diagrams. 10

14. (a) What is FPGA ? What are the components of an FPGA ? Discuss each of them in detail. Draw the structure of SRAM-based FPGA and explain its operation. 12

(b) Discuss a comparative study between FPGA, ASIC and CPLD. 8

15. (a) Draw the block diagram of 8255 PPI. Describe about each section of the block diagram and signals associated with them. 8

(b) Explain about various modes of operation of 8255 PPI. Also state the specifications of the control word to be written in a control register for configuring the device. 7

(c) Write short notes on *any one* of the following : 5

(i) VHDL

(ii) BICMOS Technology.
