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ELECTRONICS 2011

FIRST PAPER

Full Marks : 200

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. *(a)* At equilibrium, the Fermi level cannot vary spatially in semiconductor. Justify. 5

   (b) Explain how the depletion region gets formed in an unbiased *p-n* junction. Give justification in support of the word 'depletion' attributed to this particular region. 7

   (c) Describe the Hall effect. What properties of a semiconductor are determined from Hall effect experiment? 4+4=8

   (d) What is Stick diagram? Explain briefly with example. 5

2. *(a)* Discuss the physics behind the two principal breakdown mechanisms of a *p-n* junction. 10

   (b) Consider an Al-Si Schottky barrier diode. The doping concentration within the silicon is 10^{15} cm^{-3}. The effective

density of states N_c is $3 \cdot 22 \times 10^{19}$ cm^{-3} and the Schottky barrier height is 0·72 eV.

(i) Determine the built-in voltage. 5

(ii) Determine the depletion width in equilibrium. 5

(c) Plot the minority carrier current components and the total current in a p-n junction diode as a function of the distance from the junction. 5

3. (a) Consider a resistive load inverter circuit with $V_{DD} = 5$ V, $K'_n = 20\ \mu A / V^2$, $V_{IO} = 0 \cdot 8$ V, $R_L = 200$ kΩ and $W / L = 2$. Calculate the critical voltages V_{OL}, V_{OH}, V_{IL} and V_{IH} on the V_{TC}. Also find the noise margin. 10

(b) Suppose two MOS capacitors have been given to you—one having inversion layer of electrons and the other having inversion layer of holes. Explain by giving necessary energy-band diagrams how these inversion layers are created. 10

(c) For a MOS capacitor, calculate the ~~maximum space~~ charge width at temperature $T = 300$ K.

Given, acceptor concentration $N_a = 10^{16}$ cm^{-3}; intrinsic carrier concentration $n_i = 1 \cdot 5 \times 10^{10}$ cm^{-3} and the semiconductor is silicon. 5

(Continued)

4. *(a)* Explain the process of ion implantation and photolithography with necessary diagrams. 15

(b) Giving the circuit diagram for the fixed-current bias and collector-to-base bias, explain why bias stability is better in collector-to-base bias compared to that in fixed bias. 5

(c) Explain how a MOSFET can be used as a load. 5

5. *(a)* Calculate suitable resistor values for the common-emitter amplifier in Fig. 1 below. Also determine suitable capacitor values for the circuit cutoff frequencies to be 100 Hz (lower cutoff frequency) and 50 kHz (upper cutoff frequencies).

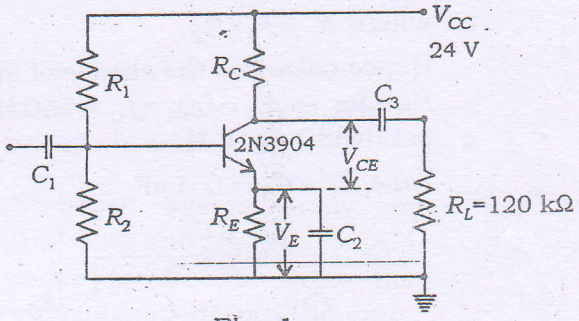


Fig. 1

Take, $V_E = 5\,V$
$V_{CE} = 3\,V$
$h_{fe} = 100$ and $h_{ie} = 1\,k\Omega$ 15

(b) Draw the circuit diagram of a MOSFET NOT gate and explain its operation. 10

6. (a) For the resonant circuit given in Fig. 2, the transfer function is

$$A_v(s) = \frac{(R/L)A_0 s}{s^2 + s(R/L) + (1/LC)} = \frac{(\omega_0/Q)A_0 s}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

where $\omega_0^2 = \frac{1}{LC}$, $f_0 = \frac{\omega_0}{2\pi}$ is the resonant frequency, Q is the quality factor, $s = j\omega$, A_0 is voltage gain at f_0.

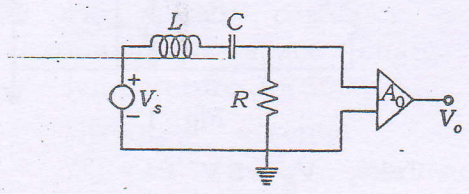
For the active resonant filter circuit (without an inductor) as shown in Fig. 3, the transfer function is

$$A_v(s) = \frac{-\frac{s}{R_1C_1}}{s^2 + \frac{C_1 + C_2}{R_3C_1C_2}s + \frac{1}{R'R_3C_1C_2}}$$

where $R' = R_1 || R_2$.

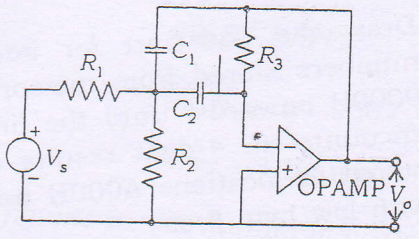
Hence calculate the values of R_1, R_2 and R_3 for $-A_0 = 50$, $f_0 = 160$ Hz, 3 dB bandwidth = 16 Hz.

Take $C_1 = C_2 = 0 \cdot 1\,\mu F$



(A resonant circuit)

Fig. 2



(An active resonant filter without an inductor)

Fig. 3 20

(b) Define sheet resistance. How is it measured? 5

7. (a) Explain the architecture of any microprocessor with neat diagram. Discuss briefly about each section. 10

(b) Classify Intel 8085A instructions into various groups with necessary examples. 7

(c) What are the general purpose and special purpose registers in Intel 8085A? Discuss in brief. 8

8. (a) In an 8085-based system, only an 8K × 8 EPROM chip and an 8K × 8 RAM chip are to be interfaced. Draw the complete interfacing circuit diagram with 8085 microprocessor, such that starting addresses assigned to EPROM and RAM chips are 0000H and 8000H respectively. Show the address map. 10

(b) Draw the block diagram of 8255 PPI chip and explain each section clearly. Also discuss about various modes of operation of 8255. 8

(c) Draw the flowchart for adding BCD numbers stored from memory location 9000H onwards, until the first zero is encountered. 4-digit results are to be stored in locations A000H and A001H with low byte first. 7

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