Total No. of Printed Pages—7

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2006

ELECTRONICS

FIRST PAPER

Full Marks : 200

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. *(a)* Consider a piece of uniformly doped germanium with 10^{15} cm^{-3} shallow acceptors. Calculate the temperature for which the electron density equals the ionized acceptor density. Ignore the temperature dependence of the energy bandgap and use $E_g = 0 \cdot 67$ eV. 10

(b) Consider a silicon metal-semiconductor junction with an *n*-type doping given by

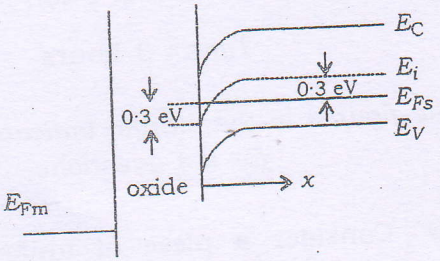
$$N_d = N_o \frac{x}{d} \quad \text{for} \quad x < d$$

$$N_d = N_o \quad \text{for} \quad x > d$$

Calculate the voltage and the capacitance corresponding to a depletion layer width of $2d$. Use $N_o = 4 \times 10^{16}$ cm^{-3}, $d = 400$ nm, the area $= 10^{-4}$ cm^{-2} and $\phi_t = 0 \cdot 8$ V. 10

(Turn Over)

2. A MOS capacitor is made from Si. When V_G is applied to the gate of the capacitor, the band diagram looks as shown below. Oxide and metal parts are not shown. Answer the questions :



(a) Is the applied voltage V_G positive or negative? Explain.

(b) Is the semiconductor *p*-type or *n*-type? What is the doping concentration?

(c) Calculate the number of electrons and holes in the bulk of the semiconductor.

(d) Calculate the number of electrons and holes near the surface of the semiconductor.

(e) Is the semiconductor under depletion, inversion or in flat-band condition? 25

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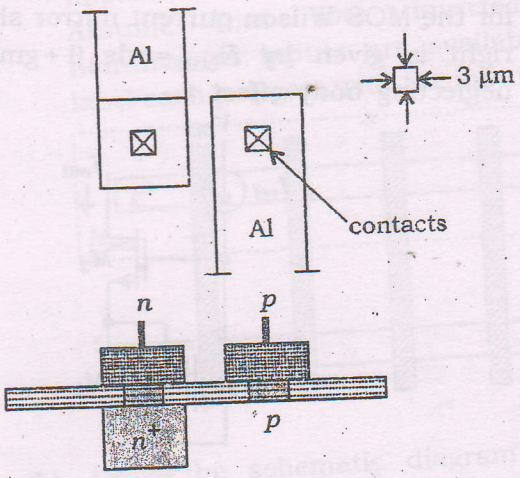
3. The mask set for a simple rectangular p-n junction diode is shown below. The diode is formed in a p-type substrate :



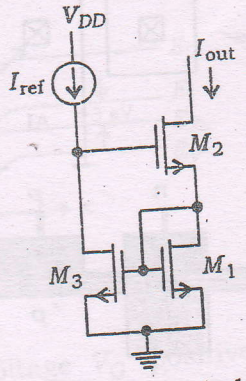
(a) How many masks are required to fabricate the structure as shown?

(b) Draw a picture of the layout for the diode, which results when a worst-case misalignment of 3 μm occurs in x-direction on each mask level. Assume that the contact level is aligned to the diffusion level and the metal level is aligned to the contact level.

(c) What will happen, if the contact hole is 6 μm × 6 μm square? Will the device work?

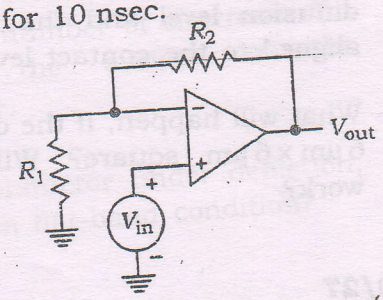
15

4. Use the small-signal model and nodal analysis to show that the output impedance for the MOS Wilson current mirror shown at right is given by $R_{out} \approx rds_2(1 + gm_2\, rds_3)$, neglecting body effect : 30



5. *(a)* For the circuit shown below, find the minimum DC open-loop op-amp gain required in order for the closed-loop gain to be accurate within 0·5%. Use $R_1 = 1\ k\Omega$, $R_2 = 19\ k\Omega$. 10

(b) If the op-amp has a unity gain bandwidth of $f_T = 1\ GHz$, find the % settling error if the op-amp is allowed to settle for 10 nsec. 10



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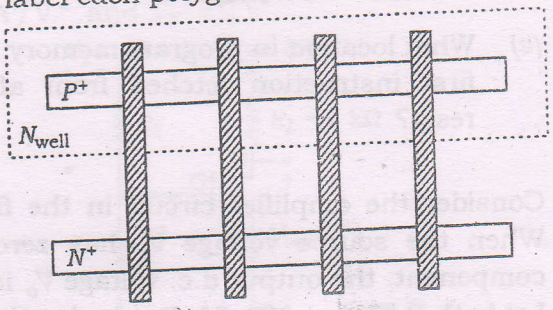
6. *(a)* On the layout diagram below, indicate the metal connections required to implement the function $F = A \oplus B$. Assume that both inverted and non-inverted inputs are available and label each polygate with the input used : 15



(b) Draw the schematic diagram for the logic gate above. 15

7. *(a)* All microprocessors have something that is called a program counter. What is this?

(b) Give the machine code as a 4-digit hex value for the instruction :

bsf 0×14F,4

(c) Whether the machine code 0×31F2 represents instruction? (Use w or f for the destination, and ACCESS or BANKED to represent the value of a bit.)

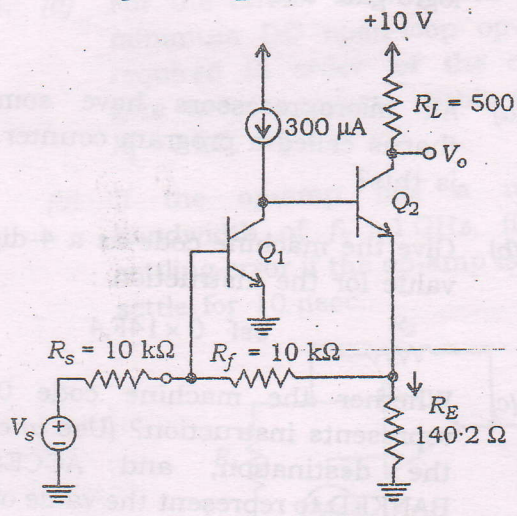
(d) For a 20 MHz clock, how long does it take to execute the following instructions? (Give the answer in microseconds.)

movff 0×230, 0×110

clrf 0×002, f

(e) What location in program memory is the first instruction fetched from after a reset? 20

8. Consider the amplifier circuit in the figure. When the source voltage V_s has zero d.c. component, the output d.c. voltage V_o is 5 V. Let both BJTs have $\beta = 50$. Determine the d.c. voltages at all the nodes and the d.c.emitter currents of Q_1 and Q_2 : 20



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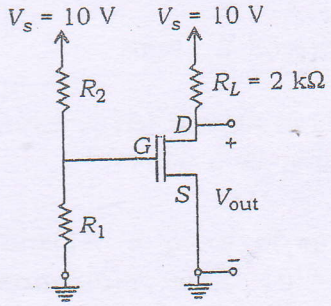
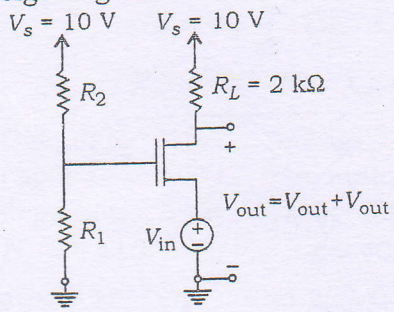
9. In the saturation region, the MOSFET shown in the circuit below has an i_D-v_{DS} relation given by $i_D = \frac{K}{2}(v_{GS} - V_T)^3$, where $K = \frac{1}{2}$ mA/V^3 and $V_T = 2$ V.



Find the relation between R_1 and R_2 that will fix the output bias voltage at 6 V. 10

10. A small source is added to the circuit above as shown in the figure. Draw a small-signal model for the circuit that can be used to analyze the gain $G = V_{out}/V_{in}$ and calculate the small signal gain : 10



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